A 3 TO 30 MHZ HIGH-RESOLUTION SYNTHESIZER CONSISTING OF A DDS, DIVIDE-AND-MIX MODULES, AND A M/N SYNTHESIZER

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Abstract

A 3 to 30 MHz synthesizer is described that uses divide and mix modules to clean up the output of a DDS resulting in a building block signal source that generates an output at 10.7 MHz with a 4.2% tuning range. The divide and mix modules are based on a previously described narrowband design that has been modified for greater tuning range. Both the old and new designs exploit inexpensive ceramic filters that are normally used in the IF stages of radio receivers. The basic 10.7 MHz band is applied to an M/N synthesizer to produce an output band from 3 to 30 MHz. Various techniques for filtering harmonics from the frequency divider output are discussed, as well as circuit design details of the 10.7 MHz mixers and filters. A PLL version of the M/N synthesizer is described that covers the band from 240 to 700 MHz, again starting from the 10.7 MHz input.

Introduction

A narrow band synthesizer using divide and mix modules based on 10.7 MHz ceramic filters previously described had the capability of extremely good spectral purity and high resolution [1]. This is in contrast to fractional N techniques, which have limited resolution; and DDS techniques, which have limited spectral purity. However, the architecture was limited to applications requiring a very small tuning range.

The divide and mix modules had input and output frequencies in the vicinity of 10.7 MHz to allow them to be cascaded, with each having typically a 10 MHz reference frequency input. The narrow bands of frequencies available at the output of the final divide and mix module needed to be centered at frequencies that were offset from the reference by a submultiple of the reference. For example, with a 10 MHz. reference, and an offset of $\frac{1}{15}$ of the reference, the center frequency is $10\frac{10}{15}$, i.e.: $10\frac{2}{3}$ MHz. Similarly, $10\frac{10}{14}$, i.e.: $10\frac{5}{7}$ MHz is also possible.

In figure 11 of [1], a scheme is shown for generating the particular frequency used for exciting cesium atoms. Of interest here is the fact that it depended on generating the frequency 10.714023 MHz, which is slightly different from 10.7142857... = $10\frac{5}{7}$ MHz. The 263 Hz difference far exceeds the tuning range of the synthesizer. The solution, shown here in simplified form in fig. 1, was to cascade two modules having a "natural" frequency of $10\frac{5}{7}$ MHz (i.e.: ÷15) following a module having a "natural" frequency of $10\frac{2}{3}$ MHz (i.e.: ÷16.)

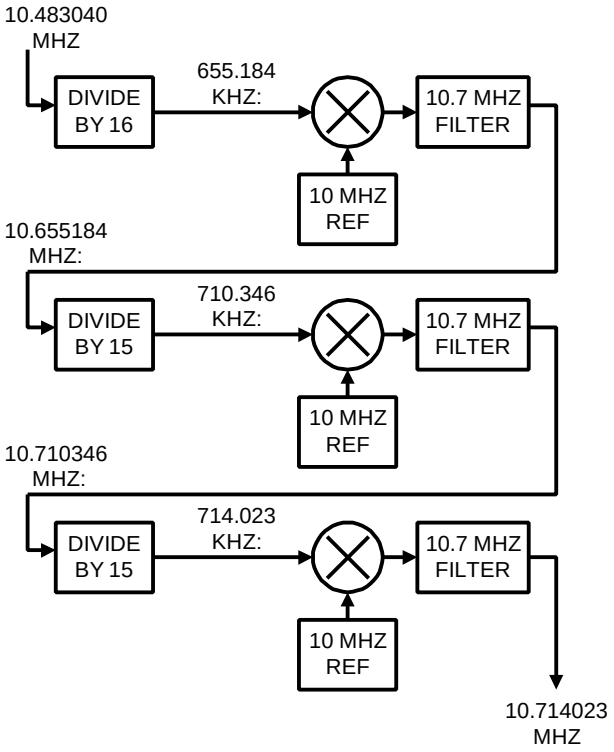
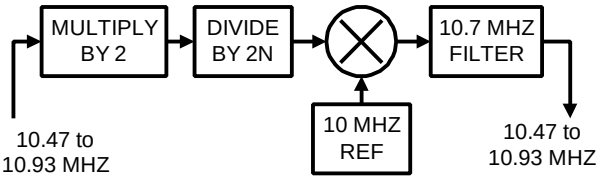


Fig. 1. Cesium architecture of [1].

Enhanced divide and mix modules

This raises the question as to what other frequencies might be generated this way by fortuitious combinations of divide ratios. The ceramic filters (described below) have a usable bandwidth of 10.47 to10 10.93 MHz, hence both the input and output frequencies of the modules are constrained to lie in this band. For division by values of N from 12 to 23, a non contiguous set of frequency bands can be generated that yield over 50% coverage of the 10.47-10.93 MHz band For example, if N=16, then the input band of 10.47-10.93 MHz is compressed into an output band of 10.654 to 10.683 MHz The >50% coverage could be increased to 100% if N were allowed to take on the in-between values of 11.5, 12.5, 13.5 ... 20.5, 21.5, 22.5. This fractional N division can be accomplished best by first multiplying the frequency by 2, then dividing by 2N. This scheme is shown in fig. 2.



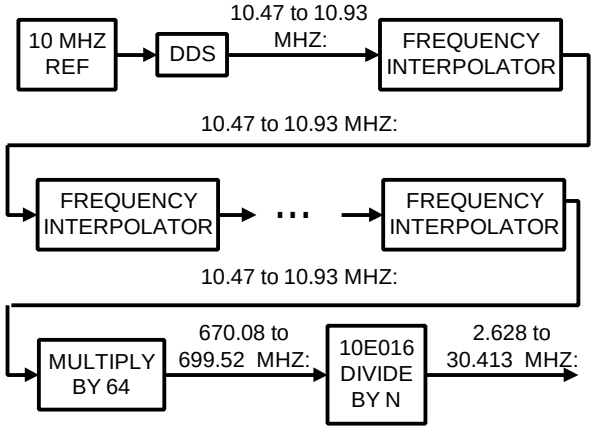
2N:	Freq. range:	2N:	Freq. range:	2N:	Freq. range:
47	10.446-10.465	38	10.551-10.575	29	10.723-10.753
46	10.456-10.475	37	10.566-10.590	28	10.748-10.780
45	10.466-10.485	36	10.582-10.607	27	10.776-10.809
44	10.476-10.496	35	10.599-10.624	26	10.806-10.840
43	10.487-10.508	34	10.616-10.642	25	10.838-10.874
42	10.499-10.520	33	10.635-10.662	24	10.873-10.910
41	10.511-10.533	32	10.655-10.683	23	10.910-10.950
40	10.524-10.546	31	10.676-10.705		
39	10.537-10.560	30	10.688-10.728		

Fig. 2. Wideband frequency interpolator.

Any number of these frequency interpolator modules can be cascaded in order to get sufficient spectral purity and/or resolution. The scheme for choosing the value of N for each module is as follows. The final module output frequency will lie in one or two of the bands shown in the table in fig. 2. One or two values of N for the final module can then be determined from the table. Knowing N, it is then possible to determine the input frequency corresponding to the desired output frequency. This input frequency is then the output frequency for the second to last module. The process can then be repeated to find the value of N and input frequency for this module. Working backward through the modules, eventually the input frequency of the first module is determined, and the DDS is set to this first input frequency as described. For example, to generate 10.808 MHz, the DDS is set to 10.868 MHz and followed by three interpolator modules having values of N of 13, 21.5, and 13, and generating frequencies of 10.836, 10.504, and 10.808 MHz respectively. As before, each module improves spectral purity by at least 22 dB. and increases resolution by over an order of magnitude. This permits continuous, high-resolution coverage of the 10.47 to 10.93 MHz band.

M/N Synthesizer

The 10.47 to 10.93 MHz front end can be used as a drive source for an M/N synthesizer to generate 3 to 30 MHz as shown in fig. 3. The input frequency is multiplied by 64 using six cascaded frequency doublers resulting in an output frequency band of 670.08 to 699.52 MHz. The frequency in this band is then divided by an integer between 23 and 255 using a commercially available IC with a guaranteed clock rate of 700 MHz.



N:	Freq. range:	N:	Freq. range:	N:	Freq. range:
255	2.628-2.743	88	7.615-7.949	35	19.145-19.986
248	2.702-2.820		...	34	19.708-20.574
240	2.792-2.914	50	13.402-13.990	33	20.306-21.197
232	2.889-3.015	48	13.960-14.573	32	20.940-21.860
	...	46	14.567-15.206	31	21.616-22.565
200	3.351-3.497	45	14.891-15.544	30	22.337-23.317
192	3.490-3.643	44	15.230-15.898	29	23.107-24.121
184	3.642-3.801	43	15.584-16.267	28	23.932-24.982
180	3.732-3.886	42	15.955-16.655	27	24.818-25.908
176	3.808-3.974	41	16.344-17.061	26	25.773-26.904
	...	40	16.752-17.488	25	26.804-27.980
100	6.701-3.497	39	17.182-17.936	24	27.920-29.146
96	6.980-7.286	38	17.634-18.408	23	29.134-30.413
92	7.284-7.603	37	18.111-18.905	N/A	30.413-30.459
90	7.446-7.772	36	18.613-19.431	22	30.459-31.796

Fig. 3. M/N synthesizer and drive source.

This results in a series of overlapping output frequency bands giving continuous coverage from 2.628

to 30.413 MHz. Divide ratios below 23 generate non-contiguous bands above 30 MHz that may be useful in certain applications. Additional frequency dividers can be cascaded to generate frequencies below 2.7 MHz.

Output harmonic filtering techniques

The architecture of fig. 3 is sufficient to generate digital clock signals, but requires additional circuitry to add sine wave output capability. The first step is to suppress even order harmonics by reconfiguring the 700 MHz divider as a two modulus (P, P+1) prescaler followed by a divide by 2 flip flop (fig. 4), where P is $N/2$ (integer division.) For example, if N=23, P=11, and P+1=12. For odd values of N, this generates an output with a duty cycle within 2% of 50% resulting in even harmonic levels of around -25 dBc in these cases. For even values of N, the harmonic suppression is limited only by circuit balance, with typical values of -40 to -60 dBc. Note that odd values of N are only needed above 15 MHz.

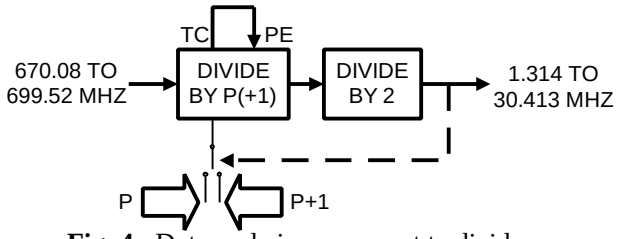


Fig. 4. Duty cycle improvement to divider.

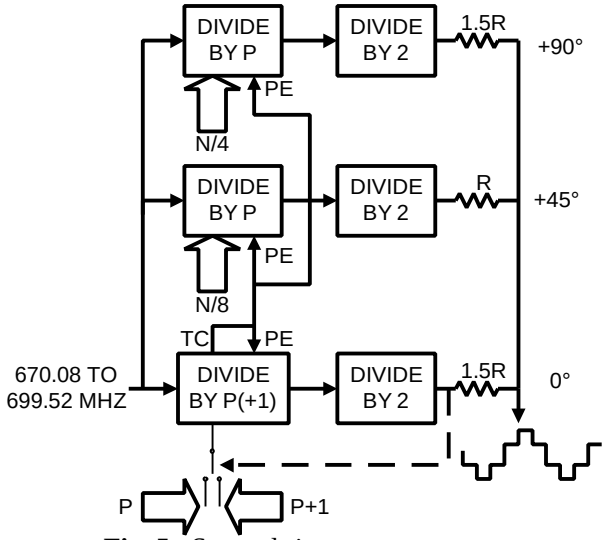


Fig. 5. Stepped sine wave generator.

It is also possible to gang together three dividers and program them to have phases spaced at approximately 45 degrees (fig. 5). They are then summed together to generate a stepped sine wave as in [2]. This suppresses the 3rd, and 5th harmonics, making filtering easier. The suppression improves as N increases. For values of N that are multiples of 8, the suppression is optimal.

Mixer circuit design

The operation of the mixer is very important to the performance of the divider and mix module. The mixer is the only source of spurious signals that cannot be filtered down to an arbitrarily low level. Hence the level of in band spurs at the output of the final mixer establishes a lower bound on the overall spur spec. Fortunately, the in band spurs are all of fairly high order, the lowest being a 12th order spur that zero beats with the desired signal at 10.909 MHz. Other in band spurs may be as high as the 22nd order one at 10.47619 MHz. According to basic mixer theory, an nth order spur should decrease in amplitude n dB for every dB decrease in the desired signal, once the signal levels are low enough for the mixer to be operating quasi-linearly.

Three different mixers were tested: the ASK-1 (+7 dBm L.O.), the SRA-3H (+17 dBm L.O.), and the M9E (+27 dBm L.O.) It was found that the rate of decrease of high order spurs as the I.F. drive level was backed off was nowhere near the value based on the order number, at least for any level likely to be used in this synthesizer. Fig. 6 shows the results for the SRA-3H for 15th order spurs. This results show that a tradeoff must be made between spur levels and phase noise floor, since phase noise will increase as the mixer drive level decreases. Another surprising discovery was that the ASK-1 attained about the same spur to carrier ratios at merely 3 dB less drive than the SRA-3H, despite the 10 dB. decrease in L.O. level. Also, the M9E wasn't significantly better than the SRA-3H, despite the 10 dB. increase in L.O. level.

Input (dBm):	Spurious level (dBc):	Input (dBm):	Spurious level (dBc):
-2	-99	-8	-112
-3	-100	-9	-115
-4	-103	-10	-117
-5	-104	-11	-120
-6	-107	-12	-124
-7	-109	-13	-126

Fig. 6. Mixer spurious levels

Putting resistive attenuators on the mixer ports to assure that they were matched with a 50 ohm system impedance didn't help the mixer performance. Another interesting phenomenon is that if the mixer is connected directly to the ceramic filter, its apparent conversion loss decreases by 3 dB compared to a 50 ohm load. This is

believed to be due to the fact that the 9.03 to 9.53 MHz image is reflected back to the mixer by the high input impedance of the filter at that frequency. This decrease in conversion loss compensates in part for the filter insertion loss, so the optimum architecture appears to be to have the filter immediately following the mixer and before any amplifier. This also has the advantage that the amplifier is only dealing with a pure sine wave and there is no chance of it generating its own intermods.

Filter circuit design

The 10.7 MHz filters are intended for use in the IF stages of direct broadcast satellite receivers and have a minimum bandwidth of 400 kHz. and a typical bandwidth of 500 kHz. Fig. 7 shows the manufacturer's recommended circuit for a single filter. It was determined experimentally that, for a single filter, this was indeed optimum for the purposes of this synthesizer. For example, it was not possible to increase the bandwidth or change the center frequency by creative use of "matching" circuitry as it is with the narrow FM broadcast type filters. Optimum coupling circuits for multiple filters with intervening amplifiers were determined experimentally as shown in fig. 7.

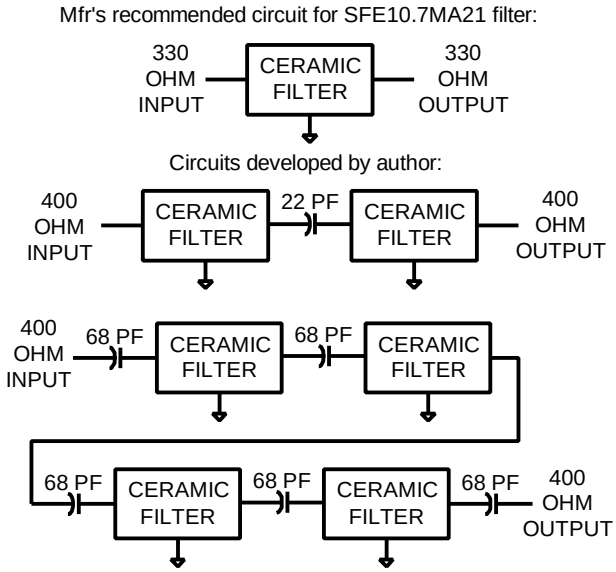


Fig. 7. Ceramic filter circuits

Up to at least four filters can be cascade. It was found empirically that when multiple filters are cascaded, the frequency response is flatter if small (less than 100 pF) capacitors are used to couple them together, rather than a direct connection. It also is helpful to raise the source and load impedances to 400 to 500 ohms. Fig. 8 and fig. 9 show the frequency response of the single filter and double filter of fig. 7.

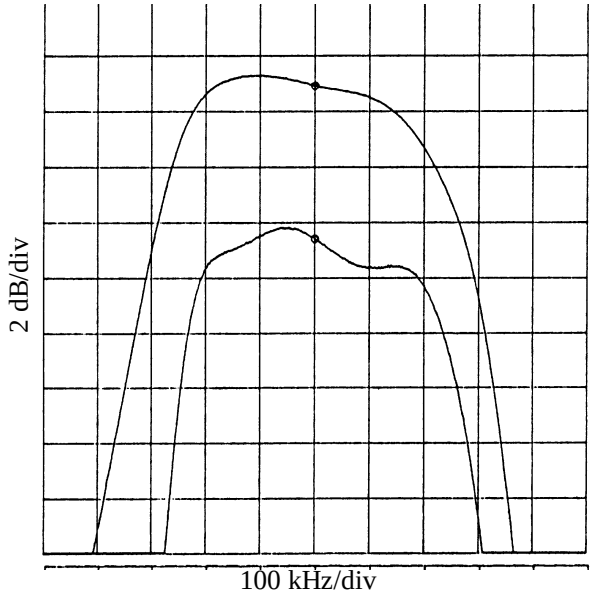


Fig. 8. Close-in selectivity of ceramic filters.

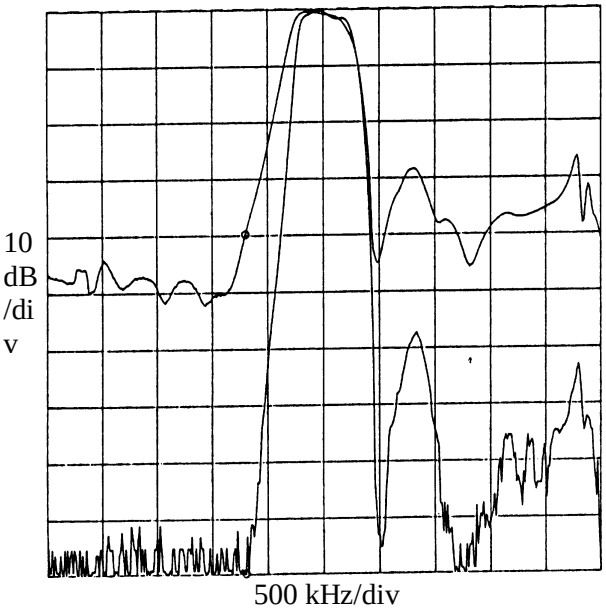


Fig. 9. Skirt selectivity of ceramic filters.

In most cases it doesn't make sense to use more than two filters because with two filters the response has already rolled off to the ultimate attenuation floor of the filters before reaching 10 MHz, where the stop band begins Also, the ultimate attenuation of two filters is 100 dB. It is unlikely that the theoretical 150 dB. for three cascaded filters would be reached in practice in a single stage because of the extraordinary shielding that would be necessary.

Figure 10 shows the overall configuration of the mixer and filter sections. The 1.8 μH. inductor and 100 pF.

capacitor combination forms a 50 ohm to 400 ohm matching network. A third ceramic filter at the output was added to remove harmonics generated in the amplifiers and also to give additional spur reduction. The signal out of this filter drives the frequency doubler in the next module or the beginning of the X64 multiplier. The doublers are of a conventional design.

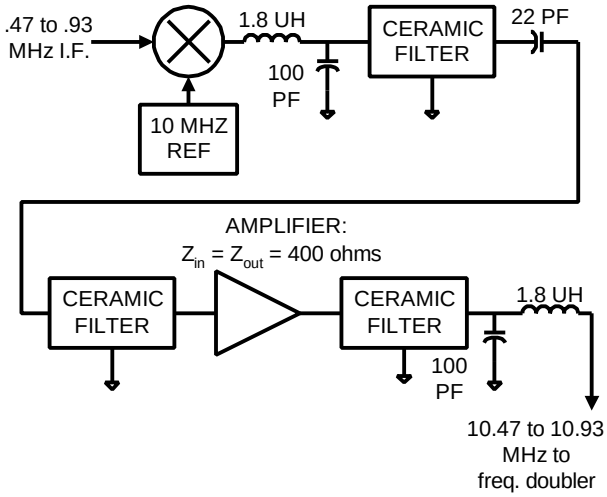


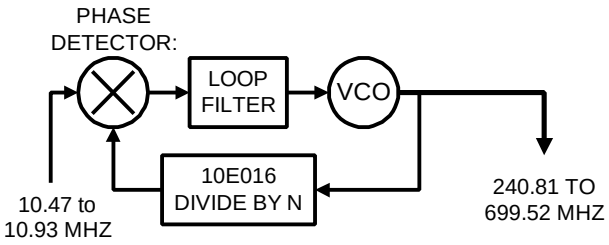
Fig. 10. Mixer and filter configuration.

It was found that the presence of second harmonic energy at the input to the doubler degraded the suppression of fundamental and third harmonic signals at the output of the full wave rectifier.

The programmable divider was connected by selector switches to one of a set of three, ⅓ octave bandpass filters used to suppress harmonics of the IF signal. As explained in [1], high order harmonics of this signal, if present, would cause spurious signals in the mixer output. An experimental synthesizer was constructed that was able to achieve a phase noise floor of less than -140 dBc/Hz with less than -110 dBc spurs. The spurs probably could have been somewhat lower if better shielding had been used.

A PLL type M/N synthesizer

Another way the 10.47 to 10.93 MHz output can be used is to shown in fig. 11. The X64 multiplier can be replaced by a PLL type multiplier using the same 700 MHz programmable counter that was used before in fig. 3. If the VCO has sufficient tuning range, the multiplication factor can be programmed over the range of 23 to 65 giving continuous tuning from 240.81 to 700 MHz. (In practice, several VCO's would probably be used to cover the range). This octave plus band can be divided down or multiplied up by powers of 2 to get continuous coverage over any desired frequency range. The phase detector reference frequency in excess of 10 MHz allows the PLL multiplier to have excellent spectral purity.



N:	Freq. range:	N:	Freq. range:	N:	Freq. range:
22	230.34-240.46	37	387.39-404.41	53	554.91-579.29
N/A	240.46-240.81	38	397.86-415.34	54	565.38-590.22
23	240.81-251.39	39	408.33-426.27	55	575.85-601.15
24	251.28-262.32	40	418.80-437.20	56	586.32-612.08
25	261.75-273.25	41	429.27-448.13	57	596.79-623.01
26	272.22-284.18	42	439.74-459.06	58	607.26-633.94
27	282.69-295.11	43	450.21-469.99	59	617.73-644.87
28	293.16-306.04	44	460.68-480.92	60	628.20-655.80
29	303.63-316.97	45	471.15-491.85	61	638.67-666.73
30	314.10-327.90	46	481.62-502.78	62	649.14-677.66
31	324.57-338.83	47	492.09-513.71	63	659.61-688.59
32	335.04-349.76	48	502.56-524.64	64	670.08-699.52
33	345.51-360.69	49	513.03-535.57	65	699.52-700.00+
34	355.98-371.62	50	523.50-546.50	(Note: 700 MHz	
35	366.45-382.55	51	533.97-557.43	is spec. limit of	
36	376.92-393.48	52	544.44-568.36	10E016 divider.)	

Fig. 11. PLL M/N synthesizer scheme.

References

[1] R. K. Karlquist, "A Narrow Band High-Resolution Synthesizer Using a Direct Digital Synthesizer Followed by Repeated Dividing and Mixing," in Proceedings of the 1995 IEEE Frequency Control Symposium, 31 May-2 June, 1995, pp.217-235.

[2] R. K. Karlquist, "A New RF Architecture for Cesium Frequency Standards," in Proceedings of the 1992 IEEE Frequency Control Symposium, 27-29 May 1992, pp. 134-142.